Amendments to the Claims

1. (Currently amended) A method for generating multiplier coefficients for a (1:m) mixer, comprising the steps of:

(a) performing recursive calculation of a multiplier set (MS);

(b) selecting a multiplier group (MG) consisting of a number of multipliers from the calculated multiplier set (MS) in dependence on a predetermined signal/noise ratio (SNR_{NOM}) of the mixer; ~~and~~

(c) writing the multiplier coefficients (MC) into a memory of the mixer in accordance with the selected multiplier group (MG); and

(d) during the step of recursive calculation, after initialization of a first multiplier V_0 of the multiplier set (MS) to zero ($V_0=0$) and initialization of a second multiplier V_1 of the multiplier set (MS) to one ($V_1=1$), further multipliers of the multiplier set (MS) are calculated in accordance with the following recursion rule:

$V_{i+2} = V_i + V_{i+1}$ for all $i = 0, 1, 2 \ldots i_{max}$,

wherein the mixer comprises a 1:10 mixer.

2. (Cancelled). ~~The method as recited in claim 1, wherein the mixer comprises a 1:10 mixer, and~~

~~during the step of recursive calculation, after initialization of a first multiplier~~ $\cancel{V_0}$ ~~of the multiplier set (MS) to zero~~ ($\cancel{V_0=0}$) ~~and initialization of a second multiplier~~ $\cancel{V_1}$ ~~of the multiplier set (MS) to one~~ ($\cancel{V_1=1}$)~~, further multipliers of the multiplier set (MS) are calculated in accordance with the following recursion rule:~~

$\cancel{V_{i+2} = V_i + V_{i+1} \text{ for all } i = 0, 1, 2 \ldots i_{max}}$.

3. (Currently amended) The method as recited in ~~claim 2~~ claim 1, wherein the step of selecting a multiplier group (MG) comprises:

selecting a multiplier group (MG) from the multiplier set (MS) consisting of two multipliers (V_i, V_{i+1}), the run index i of which produces a signal/noise ratio

$(SNR) = 20 \log [(1 + \sqrt{5})/2]^2 \cdot (i + 1/2)$

that is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

4. (Currently amended) The method as recited in claim 3, wherein the step of writing the multiplier coefficients into a memory of the mixer comprises:

writing the following multiplier coefficients (MC) into the memory of the mixer:

$MC = (0, V_i, V_{i+1}, V_{i+1}, V_i, 0, - V_i, - V_{i+1}, - V_{i+1} - V_i).$

5. (Currently amended) The method as recited in ~~claim 2~~ claim 1, wherein the step of selecting a multiplier group (MG) comprises:

selecting a multiplier group (MG) from the multiplier set (MS) consisting of three multipliers (V_i, V_{i+1}, V_{i+2}), the run index i of which produces a signal/noise ratio

$(SNR) = 20 \log [(1 + \sqrt{5})/2]^2 \cdot (i + 1)$

that is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

6. (Previously presented) The method as recited in claim 5, wherein the step of writing multiplier coefficients into a memory of the mixer comprises:

writing the following multiplier coefficients (MC) into the memory of the mixer:

$MC = (V_i, V_{i+2}, 2^* V_{i+2}, V_{i+2}, V_i, - V_i, - V_{i+2}, -2^*V_{i+2}, - V_{i+2} - V_i).$

7. (Currently amended) A method for generating multiplier coefficients for a (1:m) mixer, comprising the steps of:

(a) performing recursive calculation of a multiplier set (MS);

(b) selecting a multiplier group (MG) consisting of a number of multipliers from the calculated multiplier set (MS) in dependence on a predetermined signal/noise ratio (SNR_{NOM}) of the mixer; ~~and~~

(c) writing the multiplier coefficients (MC) into a memory of the mixer in accordance with the selected multiplier group (MG); and

(d) ~~The method as recited in claim 1,~~ wherein the mixer comprises a 1:8 mixer, and during the step of recursive calculation, after initialization of a first multiplier V_0 of the multiplier set to zero ($V_0=0$) and initialization of a second multiplier V_1 of the multiplier set (MS) to one ($V_1=1$), further multipliers of the multiplier set (MS) are calculated in accordance with the following recursion rule:

$V_{i+2} = V_i + V_{i+1}$

$V_{i+3} = V_i + V_{i+2}$

for all even-numbered $i = 0, 2, 4 \ldots i_{max}$.

8. (Previously presented) The method as recited in claim 7, wherein the step of selecting a multiplier group (MG) comprises:

selecting the multiplier group (MG) from the multiplier set (MS) consisting of two multipliers (V_i, V_{i+1}) the run index i of which produces a signal/noise ratio $SNR = 20 \log (1 +\sqrt{2}) *i$ that is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

9. (Previously presented) The method as recited in claim 1, wherein the step of writing multiplier coefficients into a memory of the mixer comprises:

writing the following multiplier coefficients (MC) into the memory of the mixer:

$MC = (0, V_i, V_{i+1}, V_i, 0, -V_i, -V_{i+1}, -V_i)$.

10. (Previously presented) The method as recited in claim 7, wherein the step of selecting a multiplier group (MG) comprises:

selecting a multiplier group (MG) from the multiplier set (MS) consisting of two multipliers (V_i, V_{i+1}) the run index i of which produces a signal/noise ratio SNR = 20 log [1 + √2] (i + 1) that is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

11. (Previously presented) The method as recited in claim 10, wherein the step of writing multiplier coefficients into a memory of the mixer comprises:

writing the following multiplier coefficients (MC) into the memory of the mixer:
$MC = (V_i, V_{i+2}, V_{i+2}, V_i, - V_i, - V_{i+2}, - V_i)$

12. (Currently amended) A method for generating multiplier coefficients for a (1:m) mixer, comprising the steps of:

(a) performing recursive calculation of a multiplier set (MS);

(b) selecting a multiplier group (MG) consisting of a number of multipliers from the calculated multiplier set (MS) in dependence on a predetermined signal/noise ratio (SNR_{NOM}) of the mixer; ~~and~~

(c) writing the multiplier coefficients (MC) into a memory of the mixer in accordance with the selected multiplier group (MG); and

(d) ~~The method as recited in claim 1,~~ wherein the mixer comprises a 1:12 mixer, and during the step of recursive calculation, after initialization of a first multiplier V_0 of the multiplier set (MS) to one (V_0=1) and initialization of a second multiplier V_1 of the multiplier set (MS) to one (V_1=1), further multipliers of the multiplier set (MS) are calculated in accordance with the following recursion rule:

$V_{i+2} = V_i + 2 * V_{i+1}$

$V_{i+3} = V_i + V_{i+1}$

$V_{i+4} = V_i + 2 * V_{i+2}$

$V_{i+5} = V_i + 3 * V_{i+1}$

for all $i = 0, 4, 8 \ldots i_{max}$.

13. (Previously presented) The method as recited in claim 12, wherein the step of selecting a multiplier group (MG) comprises:

selecting a multiplier group (MG) from the multiplier set (MS) consisting of two multipliers (V_i, V_{i+2}), the run index i of which produces a signal/noise ratio SNR = 20log $[\sqrt{2+\sqrt{3}}] \cdot (i + 2)$ that is higher than the predetermined signal/noise ratio (SNR_{NOM}) of the mixer.

14. (Previously presented) The method as recited in claim 13, wherein the step of writing multiplier coefficients into a memory of the mixer comprises:

writing the following multiplier coefficients (MC) into the memory of the mixer: $MC = (0, V_i, V_{i+2}, 2*V_i, V_{i+2}, V_i, 0, -V_i, -V_{i+2}, -2*V_i, -2*V_{i+2}, -V_i)$.

15. (Previously presented) The method as recited in claim 12, wherein the step of selecting a multiplier group (MG) comprises:

selecting a multiplier group (MG) from the multiplier set (MS) consisting of two multipliers (V_{i+3} V_{i+4}) the run index i of which produces a signal/noise ratio SNR + 20 log $[\sqrt{2+\sqrt{3}}] \cdot (i + 5)$ that is higher than the predetermined signal/noise ratio SNR_{NOM} of the mixer.

16. (Previously presented) The method as recited in claim 15, wherein the step of writing multiplier coefficients into a memory of the mixer comprises:

writing the following multiplier coefficients (MC) into the memory of the mixer: $MC = (V_i, V_{i+3}, V_{i+4}, V_{i+4}, V_{i+3}, V_i, -V_i, -V_{i+3}, -V_{i+4}, -V_{i+4}, -V_{i+3}, -V_i)$

17. (Previously presented) The method as recited in claim 1, further comprising the step of:

resolving the multipliers of the multiplier groups (MG) into Horner coefficients.

18. (Currently amended) A mixer for mixing a digital input signal with a sampled sinusoidal signal, comprising:

(a) a multiplier unit for multiplying the digital input signal by multiplier coefficients (MC);

(b) a coefficient memory for storing multiplier coefficients (MC) ~~which can be~~ are applied to the multiplier unit by means of an address generator, ~~and~~

(c) a connectable coefficient generator for generating the multiplier coefficients (MC) by recursive calculation of a multiplier set (MS) from which a multiplier group (MG) consisting of a number of multipliers is selected in dependence on a predetermined signal/noise ratio SNR_{NOM} of the mixer and corresponding multipliers (MC) are written into the coefficient memory; and

(d) wherein the mixer comprises a 1:10 mixer, and wherein the mixer is operable during a step of recursive calculation, after initialization of a first multiplier V_0 of the multiplier set (MS) to zero ($V_0=0$) and initialization of a second multiplier V_1 of the multiplier set (MS) to one ($V_1=1$), to calculate further multipliers of the multiplier set (MS) in accordance with the following recursion rule:

$V_{i+2} = V_i + V_{i+1}$ for all $i = 0, 1, 2 \ldots i_{max}$.

19. (Currently amended) A mixer for mixing a digital input signal with a sampled sinusoidal signal, comprising:

(a) a calculating circuit for calculating multipliers (MC) of a multiplier group (MG), the calculating circuit having a number of dividing circuits for dividing the digital input signal applied to an input of the mixer, and a number of switchable adders/subtractors, wherein dividing factors of the dividing circuits are Horner coefficients of the ~~resolved~~

calculated multipliers (MC) of the multiplier group (MG), and adders/subtractors are controlled in dependence on a first control bit (SUB/ADD) read out of a memory of the mixer;

(b) a demultiplexer for switching through a zero value or the multipliers (MC) calculated by the calculating circuit in dependence on a second control bit (zero) read out of the memory; and

(c) a sign circuit for outputting the positive or negative value switched through by the demultiplexer to an output of the mixer in dependence on a third control bit (SIGN) read out of the memory.

20. (Previously presented) The mixer as recited in claim 19, wherein the dividing circuits comprise shift registers.

21. (Previously presented) The mixer as recited in claim 19, further comprising: an address generator for reading out the control bits from the memory.

22. (Previously presented) The mixer as recited in claim 21, wherein the memory comprises a read-only memory (ROM).

23. (Previously presented) The mixer as recited in claim 21, wherein the memory is programmable.